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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,217	05/08/2001	Mohammad Abdallah	42390P5193C	3800

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,217	ABDALLAH ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 10,30 are rejected under 35 U.S.C. 102(e) as being anticipated by Fischer (patent No. 6,470,370)

4. Fischer taught the invention as claimed including a data processing ("DP") system comprising:

a) Memory to store a first packed data operand and second packed data operand (e.g., see col. 8 lines 43-65);

b) Partial width packed data instructions (150,155,160,165,170,175,180,185) to indicate a first packed data operand and a second packed data operand and a first operation to be performed on the subset of the corresponding pairs of data elements of

the first and second data operands (e.g., see fig.1, 2A, 4, 5, and col. 7, lines 8-65, and col. 11, lines 19-col. 12, line 24).

c) Decoder (140) coupled to partial with packed data instruction and to decode the partial-width packed data instruction (e.g., see col. 7, lines 8-55);

d) Partial width execution unit (142) coupled with the decoder to execute the operation on the subset of the corresponding pairs of data elements (e.g., see fig.1 and col. 7, line 8-col. 8, line 57).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 11-29,31,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer (patent No. 4,470,370) in view of Peleg (patent No.6, 385, 634).

7. Fischer taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Memory to store a first packed data operand and second packed data operand (e.g., see);

b) Partial width packed data instructions (150,155,160,165,170,175,180,185) to indicate a first packed data operand and a second packed data operand and a first operation to be performed on the subset of the corresponding pairs of data elements of the first and second data operands (e.g., see fig.1, 2A, 4, 5, and col. 7, lines 8-65, and col. 11, lines 19-col. 12, line 24);

c) Decoder (140) coupled to partial with packed data instruction and to decode the partial-width packed data instruction (e.g., see col. 7, lines 8-55); and

d) Partial width execution unit (142) coupled with the decoder to execute the operation on the subset of the corresponding pairs of data elements (e.g., see fig.1 and col. 7, line 8-col. 8, line 57).

8. Fischer taught instruction and microinstructions for performing operations on data elements of plural operands (e.g., see col. 25, line 1-col. 26, line 40). Fischer did not expressly detail (claims 11,20,23,26,31) decoding the partial width instruction to produce a microinstruction that corresponds to a first subset of at least one corresponding pair of data elements and a second packed data operands and a second microinstruction that corresponds to a second subset of at least one corresponding pair of data elements of the first and second packed data elements. Peleg however taught microinstructions (e.g., see col. 7, lines 34-51) that were produced and used to

individually perform operations to corresponding subsets elements of operands in the packed data operands (e.g., see col. 19 lines 1-57), and Peleg also taught parallel multipliers and adders that executed multiplications on the corresponding elements in parallel and then performing addition of corresponding results in parallel (e.g., see fig. 8 and col. 5, line13-col. 7, line 25).

9. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Fischer and Peleg. Both references were directed toward the problems of processing multiple operations using packed data. However the addition of the Peleg teachings of the separate microinstructions to implements operations on individual pairs of elements of the operand would have provided increased ability of the Fisher system to perform multiple processes on multiple pairs of data.

10. As to the limitations of claim 12, 15 the configuration of the apparatus in figure 8 of Peleg provided for the separate sending of subsets of data to individual multipliers or adders. The receipt of the data at the adders and multiplier would have necessarily been received via separate port means (i.e., input to the adders and multipliers). Peleg also taught the prior art used multiple port memories for multiply accumulate operations and that multi-ported was incompatible with the use of packed data (e.g., see col. 3, lines 51-67). Therefore the Peleg packed data system would have comprised a single ported memory and consequently would have only been able to transfer one data element at a time. As per claim 13,20,29, it would have been obvious to one of ordinary skill that on the multiply accumulate operation that did not require all elements to be used in this case the second micro-operation would have been deleted; and when an

error has occurred the micro-operation would it have been eliminated (at least to correct the error to repeat the operation correctly). Also, (claims 13,17, 21, 25, 27) Fischer taught clearing a location and therefore would have set the location to a predetermined value (i.e., zero)(e.g., see fig.10). Further (as per claim 14,16,29,32) at least because the Peleg memory (as discussed above) would have been single ported then one of the parallel operations would have been required to wait for the other operation because they would have been loaded sequentially.

11. As to claims 19,22, Fischer taught the operands being 64-bit broken into 32-bit elements (e.g., see col. 3, lines 15-33). Fischer also taught that the system was not limited to the 64-bit teaching (e.g., see col. 4, lines15-33, and col. 6, lines 35-49). Therefore since the expansion of the word width would have been well known to occur with expansion of the binary word width. Therefore since the next step in expansion from 64-bit word would have been to 128-bits. Therefore use of the 128-bit operand in the Fisher and Peleg system would have been obvious to one of ordinary skill.

12. As to claim 18, the synchronous performance of instructions on the half cycle was well known in the DP art at the time of the claimed invention. Further, as to claim 29, Fisher taught writing the results of the operations to a result register (280)(e.g., see fig.6 and 2B).

13. As per claim 24, the manner in which the microinstructions are coded was not specified in the cited prior art. However the copying of data that would have been redundant particularly in expanding packed data was well known in the DP art at the time of the claimed invention. Therefore in since the operation contained in the Fischer

and Peleg reference comprised redundant or similar operation then it would have been obvious to one of ordinary skill that to production of the similar microinstruction from a packed data instruction would have comprised replicating similar microinstructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-305-3900.

EC
April 4, 2003

ERIC COLEMAN
PRIMARY EXAMINER